TITLE OF THE INVENTION

[0005] METHOD OF FABRICATING SEMICONDUCTOR DEVICE FOR PREVENTING CONTAMINATING PARTICLE GENERATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0010] The present invention relates to a method of fabricating a semiconductor device, and more specifically, to a fabrication method that is capable of preventing particle generation at a thick deposit layer remaining at a dead zone region corresponding to an edge of a wafer after a planarization process is performed.

2. Description of the Related Art

[0015] The elements of a semiconductor device are becoming more densely integrated with finer and finer patterns to improve the processing speed and other performance parameters. As a result, manufacturing processes and mass production techniques are becoming increasingly sophisticated in order to produce these finer, highly integrated patterns for the semiconductor devices.

[0020] One process among the many manufacturing process steps involves the intermediate planarization of the multiple layers comprising the semiconductor device. For example, a chemical mechanical polishing (CMP) process and a pad poly process make it possible to improve the flatness and uniformity of silicon oxide layers within

the semiconductor device. However, these processes have some problems and drawbacks.

[0025] For example, the CMP process may cause fine scratches or generate particles that can degrade the performance or contaminate the device. The pad poly process may cause fluid particle contamination due to the employment of a sacrificial oxide etch process followed by the use of the poly pad.

[0030] The ability to control particle contamination during the manufacturing process is indispensable to ensure the proper functioning of the semiconductor devices, and to improve production yields. However, it is not always easy to determine the precise source of the particles.

[0035] In one particular case of particle contamination, it has been observed that particles are moved from an edge of a wafer toward a pattern on the wafer. A main component of the particles is a silicon substance, such as silicon (Si) or silicon dioxide (SiO_2). As can be expected, finding the source of the silicon contamination is an extensive process and not easily deduced, given that many elements in the semiconductor field are comprised of silicon (Si) or SiO_2 type materials.

[0040] For example, the following elements are likely sources of Si or SiO_2 particle generation at an edge of a wafer: a quartz bath and a quartz robot arm used in a wet bath, a quartz tube and a quartz boat used in a diffusion process, a focus ring, a shadow ring and a shower head of silicon or quartz used in a dry etch process, and

slurry used as a polishing source in a CMP process. Moreover, since the wafer itself is made of Si, SiO_2, SiN, etc., it may be also a source of particle contamination due to scratching or chipping.

[0045] The chemical mechanical polishing (CMP) process is widely used in the semiconductor manufacturing field for horizontally planarizing various kinds of layers, such as oxide layers, nitride layers, metal layers and the like, which are sequentially deposited on the semiconductor wafer to form the integrated circuits.

[0050] In a CMP process, a polishing support table is used for supporting and rotating a CMP pad positioned on the table. A wafer confronts the CMP pad, and is fixed and rotated by a carrier, which moves vertically to selectively contact the CMP pad, which CMP pad is also rotated at the same time by the table. A slurry mixture, which comprises a mixture of predetermined types of chemicals and other ingredients, is provided at the central point of the CMP pad, and then evenly distributed and coated on the upper surface of the CMP pad by the rotating force of the CMP pad. The semiconductor wafer attached to the wafer carrier selectively contacts the slurry covered CMP pad.

[0055] As a result of the relative rotation between the wafer and the CMP pad, and the slurry mixture on the surface of the CMP pad, both mechanical friction and chemical reactions take place, and the material comprising the layer to be polished is gradually removed from the surface of the wafer. As a result, a wafer is said to be

planarized to a certain pre-set thickness on the surface of the wafer.

[0060] The film polished by the CMP process is generally deposited using a chemical vapor deposition (CVD) process. During the CVD process, a film having a desired thickness is grown by a chemical reaction on the surface of the wafer, except a rear portion of the wafer. A typical CVD process produces a film on the upper surface of the wafer only, while a Low Pressure CVD (LPCVD) process allows a film to be grown on both the upper and lower surfaces of the wafer.

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[0065] Depending on the structure of the CVD apparatus, there may occur a phenomenon in which a film is grown at a dead zone region corresponding to an edge portion of the upper surface of the wafer, or at the lower surface of the wafer, and the grown film at the edge portion or lower surface of the wafer has a thickness different from that of the film formed on the upper surface of the wafer. In order to prevent the film from growing on the lower surface, a flow of N_2 gas is generally applied to the lower surface of the wafer during the deposition process. However, such a preventive measure is not feasible for application at the upper surface of the wafer considering the structure of the CVD apparatus, and thus a film of non-uniform thickness is usually deposited at a dead zone region of the upper surface of the wafer.

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[0070] FIGS. 1 to 3 are schematic views illustrating a conventional method for fabricating a semiconductor device. Referring to FIG. 1, after a film is deposited on a wafer 10, the deposited layer 20, such as an oxide layer, exhibits a tendency to have a

higher growth rate at a dead zone region 24 (see FIG. 2) corresponding to an upper sidewall or edge portion of the wafer 10, due to the characteristics of the gas flow used to form the layer.

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[0075] Thereafter, as shown in FIG. 2, a conventional CMP process is performed to planarize the deposited layer 20. Note that the planarized deposited layer 22 of the upper surface side has a uniform thickness extending nearly to the edge of the wafer, but the planarized deposited layer in the dead zone region 24, corresponding to the upper sidewall portion of the wafer 10, has a non-uniform thickness due to the inherent restrictions of the CMP process and the initial gas flow characteristics. As a result, the deposited layer on the upper side wall portion of the wafer 10 remains thicker relative to the planarized deposited layer 22 remaining on the upper surface of the wafer 10. Moreover, the slurries may accumulate at the dead zone region 24 and thus the probability of particle occurrence becomes higher. As can be seen, after the CMP process is completed, the difference in the thickness of the deposited layer 20 between the uniform planarized deposited layer 22 and the non-uniform portion at the dead zone region 24 is increased relative to the pre-planarized conditions.

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[0080] Afterwards, in order to form a pattern on the planarized deposit layer, a photolithography process and a dry etch process are sequentially performed. In the general patterning process, an edge expose wafer (EEW) process is also performed to remove the deposited layer of the exposed sidewall of the wafer 10.

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[0085] Referring to FIG. 3, since the deposited layer 20 in the dead zone region 24 was thicker than that of the planarized deposited layer 22, even after the CMP and etching processes, a residual oxide 26 still remains at the upper sidewall portion of the wafer 10. This is because the dry etch is performed with reference only to the thickness of the planarized deposited layer 22 formed on the upper surface of the wafer 10.

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[0090] Moreover, a group of cone shaped particles 28 are generated at a boundary between the removed portion of the deposited layer and the remaining portion of the deposited layer at an edge of the upper surface of the wafer 10. The group of cone shaped particles 28 comprise a silicon substance, such as silicon (Si), silicon dioxide (SiO_2), or the like.

[0095] As the deposition of a layer and the dry etch are repeated, the region comprising these cone shaped particles 28 becomes wider and wider. As a result, these particles generated at the dead zone region 24 move toward a pattern on the wafer during a wet etch process as indicated by the arrow in FIG. 3. In particular, this phenomenon frequently occurs in a wet etch process using an HF solution. For example, if a wet etch process using an HF solution is performed during a pretreatment process, many cone shaped particles 28 are generated at the dead zone region, which then separate from the boundary and are introduced into the pattern 20 along with the flow of the wet etch chemical, thereby contaminating the pattern.

These cone shaped particles 28 can grow larger and may change into spherical particles during a subsequent film deposition process.

[0100] In view of the foregoing, it is necessary to continue the efforts to identify and remove sources of particle contamination.

SUMMARY OF THE INVENTION

[0105] An object of the present invention is to provide a method of fabricating a semiconductor device that is capable of preventing particle generation and enhancing production yields by minimizing a thickness of a deposit layer remaining at a dead zone region corresponding to an edge of a wafer.

[0110] To achieve the above objects and other advantages, there is provided a method for fabricating a semiconductor device, including depositing a layer on a wafer and then planarizing the deposited layer. The resulting planarized layer has a uniform region of uniform thickness extending along a wafer surface and nearly to an edge of the wafer, and a non-uniform region of non-uniform thickness corresponding to the edge of the wafer. A photoresist layer is coated on the planarized layer, and then a portion of the coated photoresist layer corresponding to an edge region of the wafer is removed, thereby exposing at least the non-uniform region of the planarized layer. The exposed non-uniform region of the planarized layer is etched, and a remaining

portion of the coated photoresist layer on the planarized layer is stripped, thereby forming a pattern layer comprising a portion of the uniform region of the planarized layer.

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[0115] According to another aspect of the present invention, there is provided a method of fabricating a semiconductor device, including depositing a layer on a wafer, with the deposited layer having a uniform region of uniform thickness extending along a wafer surface and nearly to an edge of the wafer, and a non-uniform region of non-uniform thickness corresponding to the edge of the wafer. A photoresist layer is first coated on the deposited layer, and then a portion of the coated photoresist layer is removed, corresponding to an edge region of the wafer, thereby exposing at least the non-uniform region of the deposited layer. At least the exposed non-uniform region of the deposited layer is etched, and then the coated photoresist layer remaining on the wafer is stripped. The uniform region of the deposited layer is then planarized to thereby form a pattern layer.

[0120] In the present invention, a residual deposited layer remaining at the dead zone region of the wafer is removed prior to, or after, a planarization process is performed, resulting in a remarkable decrease in the occurrence of contaminating particles generated during the patterning processes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0125] The above objects and other advantages of the present invention will become more apparent by describing in detail the preferred embodiments thereof with reference to the accompanying drawings, in which:

[0130] FIGS. 1 to 3 are schematic views illustrating a conventional method for fabricating a semiconductor device;

[0135] FIGS. 4 to 7 are schematic views illustrating a method for fabricating a semiconductor device in accordance with an embodiment of the present invention;

[0140] FIGS. 8 to 11 are schematic views illustrating a method for fabricating a semiconductor device in accordance with another embodiment of the present invention; and

[0145] FIGS. 12A and 12B are particle maps of a wafer prepared in accordance with a process of the present invention, and a conventional process, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0150] The present invention will now be described more fully with reference to the accompanying drawings, in which a preferred embodiment of the invention is shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, the embodiments are provided so that this disclosure will be thorough and

complete, and will fully convey the concept of the invention to those skilled in the art. In the drawings, the thickness of a layer or region are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on " another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

[0155] As described above with reference to FIGS. 1 to 3, the particle contamination during the CMP process originates because of a difference in the thickness between the deposited layer on the upper surface of the wafer 10, and the deposited layer of the upper sidewall of the wafer 10 after the CMP process is performed. Thus, to eliminate the contamination problem, the present invention is broadly directed to a method of removing the deposited layer at the upper sidewall region either prior to, or after the CMP process is performed.

[0160] FIGS. 4 to 7 are schematic views illustrating a method for fabricating a semiconductor device in accordance with an embodiment of the present invention, in which the deposited layer at the upper sidewall region is removed prior to performing the CMP planarization process.

[0165] Referring to FIGS. 4 and 5, a deposited layer 20 is formed on a wafer 10. Note that the deposited layer 20 has a region of uniform thickness 20a extending along the wafer surface and nearly to the edge of the wafer 10, and a region 20b of non-uniform thickness corresponding to an upper sidewall or edge of the wafer 10.

Thereafter, a photoresist film 30 is coated on the entire deposited layer 20 with a thickness in the range of approximately 5000-15000 Å. Afterwards, an edge portion of the photoresist film 30 is removed by an edge expose wafer (EEW) process, to thereby expose at least the edge portion of the deposited layer 20 (i.e., non-uniform region 20b) as shown in FIG. 5. As also shown in FIG. 5, depending on the desired pattern, a portion of the uniform region 20a may also be exposed when the photoresist film 30 is removed.

[0170] Referring to FIG. 6, any exposed portions of the deposited layer 20, and including at least the edge portion, are removed by a subsequent conventional wet etch process. Here, the exposed non-uniform region 20b of the deposited layer 20 at the edge of the wafer 10 corresponds to the dead zone region 24 described above with reference to FIG. 2. This exposed non-uniform region 20b is thus removed prior to performing the CMP planarization process. As a result, only a deposit layer pattern 40 (corresponding to all or a portion of the uniform region 20a) remains on the upper surface of the wafer 10. Here, a target thickness of the deposit layer removed by the wet etch process is in a range of approximately 5000-15000 Å.

[0175] Referring to FIG. 7, the remaining photoresist film 30 is then stripped, leaving only the deposit layer pattern 40 remaining on the wafer 10. Thereafter, a CMP planarization process is performed to planarize the deposit layer pattern 40.

[0180] FIGS. 8 to 11 are schematic views illustrating a method for fabricating a

semiconductor device in accordance with another embodiment of the present invention, in which the deposited layer at the upper sidewall region is removed after performing the CMP planarization process.

Sub A17 **[0185]** Referring to FIG. 8, a deposited layer 20 is formed on a wafer 10. Thereafter, the deposited layer 20 is planarized and polished using a CMP process, thereby forming a planarized layer 50 as shown in FIG. 9. Note that the planarized layer 50 has a region of uniform thickness 50a extending along the wafer surface and nearly to the edge of the wafer 10, and a region 50b of non-uniform thickness corresponding to an upper sidewall or edge of the wafer 10. In the planarized layer 50, the uniform region 50a is thinner than the non-uniform region 50b.

Sub A27 **[0190]** Referring to FIG. 10, a photoresist film 30 is then coated on the entire planarized layer 50 with a thickness in the range of approximately 5000-15000 Å. Afterwards, an edge portion of the photoresist film 30 is removed by an edge expose wafer (EEW) process, to thereby expose at least the edge portion of the planarized layer 50 (i.e., non-uniform region 50b). Depending on the desired pattern, a portion of the uniform region 50a may also be exposed when the photoresist film 30 is removed.

Sub A37 **[0195]** Any exposed portions of the planarized layer 50, and including at least the edge portion, are removed by a subsequent conventional wet etch process. Here, the exposed non-uniform region 50b of the planarized layer 50 at the edge of the

wafer 10 corresponds to the dead zone region 24 described above with reference to FIG. 2. This exposed non-uniform region 50b is thus removed after performing the CMP planarization process. Here, a target thickness of the planarized layer removed by the wet etch process is in a range of approximately 5000-15000 Å.

[0200] Referring to FIG. 11, the photoresist film 30 is then stripped away, leaving only the deposited layer pattern 60 (corresponding to all or a portion of the uniform region 50a) remaining on the upper surface of the wafer 10.

[0205] According to the above-described preferred embodiments, since a thick residual of the deposited layer formed on the sidewall of the wafer 10 is eliminated either before or after the CMP planarization process is completed, it is possible to prevent the generation of contaminating particles during subsequent manufacturing processes.

[0210] FIGS. 12A and 12B are particle maps showing a distribution of particles after a subsequent process is performed on the wafer, comparing the conventional art process (FIG. 12B) in which particles are not removed prior to performing the subsequent process, and the present invention (FIG. 12A) in which particles are removed prior to performing the subsequent process.

[0215] As seen from FIGS. 12A and 12B, the wafer of the present invention in FIG. 12A exhibits remarkably fewer particles compared with the wafer of the conventional art as shown in FIG. 12B. This confirms that with the present inventive method, the

number of particles introduced into the deposit layer pattern remarkably decreases due to the removal of the deposited (or planarized) layer portion of the dead zone region of the wafer, either prior to or after the CMP planarization process.

[0220] As a result, particle generation remarkably decreases and it thus becomes possible to secure high production yields and enhance the performance of the resulting devices.

[0225] While the present invention has been described in detail, it should be understood that various changes, substitutions and alterations could be made hereto without departing from the spirit and scope of the invention as defined by the appended claims.